UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,727	03/09/2004	Larry L. Byers	MP0787	1768

26703 7590 05/21/2010

HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098

EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
05/21/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,727	BYERS ET AL.	
	Examiner	Art Unit	
	SHANE M. THOMAS	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 48-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 48-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/26/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 2/26/2010. Claims 1-7 and 48-85 remain pending.

All previously outstanding objections and rejections to the Applicant's disclosure and claims not contained in this Action have been respectfully withdrawn by the Examiner hereto.

Information Disclosure Statement

The information disclosure statement filed 2/26/2010 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because NPL items 1 and 4 do not have publication dates accompanying their respective entries in the form 1449. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Response to Amendments

As per Applicant's amendments, the Examiner offers an alternate interpretation in light of the Gary reference to teach the amended claim limitations with the addition of the previously cited Hughes reference.

Applicant argues in light of the present amendments on page 14 of the present response that claim 63 distinguishes from Gary in that the servo controller interface is connected between the servo controller and the first and second processors. As detailed in the rejection below, the Examiner has modified his mapping of the "servo controller interface" as explained in detail in the rejection below. More specifically, the Examiner is considering (1) the MUX 205 in combination with (2) the protocol logic 204, the bus wires 114, and (3) the corresponding control I/O register 203 for the servo interface, to be the "servo controller interface" as the combination of these elements interfaces between the processors 110 and 111 and the servo interface 108 and shown in figure 1.

With regard to the new amendments to claim 1, Applicant argues on page 15 of the response that the pipeline control and speed-matching modules are both directly connected to the servo controller, between the servo controller and the processors. The Examiner refers the Applicant to figures 2 and 3 of Gary. Figure 2 shows a pipeline control module 204 portion of the servo controller interface that is directly connected to the servo interface (which is one of the peripherals 202) via one of MUXes 205. Referring to figure 3, Gary teaches an I/O register 301 for buffering data between the processors and a given peripheral through the servo controller interface MUXes 205- the Examiner is considering these control or I/O registers to be part of the "interface" that interfaces between each I/O component/peripheral 202 (figure 2) and the

processors. For example, the peripheral I/O register 301 that corresponds to the servo controller 108 is considered to be part of the "servo controller interface" since this "interface" is responsible for routing data to and from the servo controller 108 from and to the processors.

The Applicant further argues on page 15 of the response that the present invention of claim 63 states that the servo controller interface does not include first or second buses or processors. This amendment is taught by referring again to figure 1 of Gary. With the Examiner considering the first and second buses to refer to each corresponding bus 102 coupled to each processor as shown and the servo controller interface to comprise the combination of (1) MUX 205, (2) protocol logic 204 (figure 2), and (3) the respective control register 203 for the servo interface, the new amendments to claim 63 as taught by Gary.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6 and 48-62 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claims 1 and 52, the limitation of "the pipeline control and the speed-matching module are directly connected to the servo controller" is not explicitly taught by the Applicant.

As shown in figures 12A(i) and 12A(ii), the pipeline controller module 1203 is clearly shown as being attached directly to the speed-matching controller, not to the servo controller 216. Further, the Examiner can find no teaching in Applicant's specification that makes optional a direct connection between the pipeline control module 1203 and the servo controller 216. As such, the amendment is considered new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6,48-50,52-57,59-61, and 63-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253) in view of Hughes et al. (U.S. Patent Application Publication No. 2002/0184453).

As per claims 1 and 52, Gary teaches an embedded disk controller (figure 1 sans elements 101 and 107) having a servo controller (combination of elements 105 and 108) the embedded disk controller comprising:

A servo controller interface (combination of {1}MUX 205 (figure 1 and 2), {2} buses 114 (figures 1 and 2), {3} logic 204 (figure 2), and {4} I/O registers 301 (figure 3, which are the control registers 203 of figure 2) - so basically the connection interface that couples processors 111 and 110 to every I/O element of figure 1, including servo controller 108) **including a speed-matching module** (I/O register 301, which stores data to and from a corresponding I/O device,

of which the servo controller 108 is one such device - [4/66 - 5/4]. The register 301 may be considered a “speed matching" module since it is used to buffered data between the domain of the servo controller and the domain of the processors, which Applicant discusses in the background section of the present invention, paragraph 16. Paragraph 16 states that data buffering is commonly used between two elements when the elements' I/O speeds are different. The same argument can be made for the operating of the processors 110 and 111 and the servo controller 108, which is why the I/O register 301 is utilized to store data to/from the processors and servo controller. Because the Applicant does not further limit the "speed module" as it is discussed in the specification (e.g. is a fifo, etc.), the I/O register 301 of Gary teaches the broadest, reasonable interpretation of a "speed matching” module as currently presented in the claim) **and a pipeline control module** (logic 204, shown in figure 2) **that a first processor and a second processor** (P0 110 and P1 111) **share memory mapped registers without conflicts** [5/10-13] and [5/29-49]. Gary teaches in section [5/10-13] that peripheral devices are shared among the processors P1 and P0, wherein each device is memory mapped to a designated address space, and wherein that range of memory mapped addresses includes identification for registers. Therefore, it can be see that because the processors share the peripheral devices without conflict and each device has its own registers that are memory-mapped, that the processors share the memory mapped registers without conflicts. The pipeline control module 204 serializes access to the devices to one processor at a time as discussed in [5/29-49].

Gary goes on to teach that **the speed matching module and the pipeline control module are directly connected to the servo controller in between the servo controller and the first processor and the second processor** (referring to figure 2 and [4/66 - 5/4] is can be

seen that the speed matching module (e.g. the I/O register 301 that corresponds to the servo controller 108) is directly connected to the servo controller since it hold data entering and leaving the servo controller, and the pipeline control module 204 is connected to the speed matching module 203 in much the same way as shown and taught by the Applicant in figures 12A(i) and 12A(ii) - via a bus 114. The two modules are between the processors and the servo controller as shown in figure 2 of Gary - the servo controller being one of the peripherals 202).

Gary teaches that the processors may be different [3/63-65] but does not specifically teach wherein the first and second processors operate at different rates. Hughes teaches a memory system where processors generally operate at different clock rates (¶3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the servo controller system of Gary with the teaching of processor cores operating at different clock cycles as taught by Hughes in order to have achieved the predictable result of the processors P0 and P1 of Gary being capable of operating at different rates.

As per claims 2,53,64,72, and 80, Gary teaches in [3/63-65] that the processors P0 and P1 may be different to optimize particular tasks. As taught above, Hughes teaches different processors within the same system operating at different clock rates. It would have been obvious to one having ordinary skill in the art to have used different processor frequencies to optimize the desired performance for the specific desired tasks.

As per claims 3 and 54, it is necessarily inherent that the bus element 114 of the service interface connecting the servo controller interface (defined supra) to the servo controller (also defined supra) operates at a given frequency. As such, claims 3 and 54 are taught since the claim only states that the servo controller and the servo controller interface must operate in the same or

different frequency domains. It follows that in order to communicate data to and from two elements, that those elements both be operating on their own frequency, and whether or not that frequency is the same is immaterial to the claim language as the two elements may be operating in difference frequencies as well. In order words, the fact that two elements can communicate implies they are operating under their own frequency, which thereby teaches the limitation.

As per claims 4,55,68, and 76, Gary teaches that the speed matching module (corresponding I/O register 301 for the servo controller 108) ensures communication without inserting wait states to the servo controller interface when writing to the servo controller - [5/29-39], where data can be written or ready from the I/O register 301 immediately by the owning processor; therefore no waiting is required.

As per claims 5 and 56, according to Gary, because of the pipeline control module 204, the processors exclusively share access to the disk drive 107 [6/55-67], and a situation cannot arise where both processors are reading from the disk drive at the same time (i.e. read conflict).

As per claims 6 and 57, the pipeline control module 204 of the servo controller interface (as defined above with respect to claims 1 and 53) comprises a hardware mechanism for indivisible register access [7/7-15] to the first or second processor. In other words, only one processor may be the owner of the peripheral's I/O register 301 (figure 1), thereby being able to access the peripheral [5/23-27].

As per claims 48,59,69,77, and 84 the pipeline control module 204 resolves conflict (simultaneous access request from both processors for the same resource) between the first and second processor transactions (for access control) [6/48-54] as the protocol logic 204 implements the dynamic sharing of the peripherals with the processors.

As per claims 49 and 60, as shown in figure 1, the first and second processor communicate with the servo controller via separate buses (both labeled 102) as shown in figure 1 - [4/2-3], as well as shown in figure 2.

As per claims 50 and 61, assuming processor P1 is the owner of a given peripheral (in this case the disk drive 107 itself), the pipeline control module 204 will hold write access to the second processor P0 until the first processor releases the peripheral from its ownership - [6/55 - 7/6].

As per claims 63,71, and 79, Gary teaches a disk controller 103 having servo controller (combination of elements 105 and 108), the servo controller interface (combination of all elements within 103 except 105 and 108) comprising:

a first interface (connection between processor 110 and bus 102) for communicating with a first processor 110 over a first bus 102 (figure 1) at a first rate (rate at which the processor is operating) and a second interface (connection between processor 111 and bus 102) for communicating with a second processor 111 over a second bus 102 (figure 1) at a second rate (rate at which the second processor is operating). Since bus 102 is separated by a MUX 205, the Examiner is considering each bus connecting a respective processor 110,111 to be a separate bus despite identical numbering. Gary further teaches the servo controller interface (combination of {1}MUX 205 (figure 1 and 2), {2} buses 114 (figures 1 and 2), {3} logic 204 (figure 2), and {4} I/O registers 301 (figure 3, which are the control registers 203 of figure 2) - so basically the connection interface that couples processors 111 and 110 to every I/O element of figure 1, including servo controller 108) selectively granting one of the first and second processors access

to a servo controller 108 (whichever processor supplies the "owner" signal - [4/37-40] and [5/28-49]).

Gary further teaches that the servo controller interface is connected and positioned between the servo controller and the first and second processors (refer to the interpretation above for the servo controller interface - it can be seen that all of the components of this interface are between the processors and the servo controller) and that the servo controller interface is directly connected to the servo controller (via the peripheral I/O register 301 - as shown in figure 3 and discussed in [4/66 - 5/2] as it hold the data entering and leaving the servo controller) and the first and second buses and the servo controller interface does not include the first and second buses and the first and second processors (refer to figure 2 and figure 3 - the defined servo controller interface couples the processors to every peripheral device, one of which includes the servo controller, and does not include processors 110 and 111 or buses 102).

Gary does not specifically teach but Hughes teaches wherein the clock rates of the processors are different. Hughes teaches a memory system where processors generally operate at different clock rates (¶3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the servo controller system of Gary with the teaching of processor cores operating at different clock cycles as taught by Hughes in order to have achieved the predictable result of the processors P0 and P1 of Gary being capable of operating at different rates.

As per claims 65,73, and 81, Gary teaches a speed matching module that resolves conflicts between at least a first and second clock domains (I/O register 301, which stores data to and from a corresponding I/O device, of which the servo controller 108 is one such device -

[4/66 - 5/4]. The register 301 may be considered a “speed matching" module since it is used to buffered data between the domain of the servo controller and the domain of the processors, which Applicant discusses in the background section of the present invention, paragraph 16. Paragraph 16 states that data buffering is commonly used between two elements when the elements' I/O speeds are different. The same argument can be made for the operating of the processors 110 and 111 and the servo controller 108, which is why the I/O register 301 is utilized to store data to/from the processors and servo controller. Because the Applicant does not further limit the "speed module" as it is discussed in the specification (e.g. is a fifo, etc.), the I/O register 301 of Gary teaches the broadest, reasonable interpretation of a "speed matching” module as currently presented in the claim).

As per claims 66,74, and 82, Gary teaches the speed matching module transitions servo controller accesses from one of the first and second clock domains (e.g. a processor 110 or 111 block domain) to the other of the first and second clock domains (to the servo controller’s clock domain). As known in the art, a buffering element from one frequency domain writes data to a buffer while the element in the second frequency domain reads the data, thereby resolving the differences between the first and second domains - such information is provided by the Applicant as well, which is discussed in the background section of the present invention, paragraph 16. Paragraph 16 states that data buffering is commonly used between two elements when the elements' I/O speeds are different.

As per claims 67,75, and 83, it can be seen that the memory mapped registers are within the servo controller 108 since Gary teaches that internal registers of the peripheral devices are

memory mapped [5/10-13] and are "shared" since only one of the processors can be the owner and access the device and its memory mapped registers at a time - [5/50-54].

As per claims 70,78, and 85, the servo controller interface, by means of the pipeline control module 204, delays a write access for one of the processors 110,111 during write conflicts. Assuming processor P1 is the owner of a given peripheral (in this case the disk drive 107 itself), the pipeline control module 205 will hold write access to the second processor P0 until the first processor releases the peripheral from its ownership - [6/55 - 7/6], thereby overcoming write conflicts.

Claims 7,51,58, and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253) in view of Hughes et al. (U.S. Patent Application Publication No. 2002/0184453), as applied to claims 6 and 57 above, in further view of Snyder et al. (U.S. Patent No. 6,745,274).

As per claims 7,51,58, and 62, Gary suggests the need for a processor that loses a race condition when vying for a common resource to be made aware that it failed to acquire the resource (to be able to reschedule the write data in one example presented by Gary) but does not specifically teach using a semaphore to control sharing access of the common resource. Snyder teaches a semaphore to synchronize access to a shared resource [1/22-25] and [2/26-38] without requiring special instructions to implement the synchronization control [8/31-36]. Further, Snyder teaches in [4/37-40] that the use of the semaphore allows for processor that did not successfully acquire the shared resource to “learn of the failure” and re-attempt to acquire the semaphore lock - thereby providing a resolution to the suggestion of Gary - [7/11-15].

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the disk controller system of Gary with the teaching of a semaphore of Snyder in order to have implemented a sharing technique that would have allowed a processor (p0, p1) of the system of Gary to have determined that it lost or did not acquire a shared resource when both processors simultaneously request access to the shared peripheral. Once the determination is made, the losing processor may vie for the semaphore lock again to access the peripheral once the other processor releases the lock (figure 2, step 200 of Snyder).

Further regarding claims 51 and 62, Snyder teaches that the hardware mechanism of the disk controller system of modified Gary can be a semaphore register [2/20-21].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fish (U.S. Patent Application Publication No. 2003/0107834) teaches using a FIFO buffer in a servo interface - figure 4 and ¶34.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANE M. THOMAS whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Shane M Thomas/
Primary Examiner, Art Unit 2186